AMENDMENTS TO THE CLAIMS:

The below listing of claims replaces all previous listings and versions of claims in this application:

1. (Currently Amended) A pseudo noise (PN) ~~PN~~ code hopping method for mitigating cross-correlation interference, the method comprising the steps of:

providing a memory device;

storing a plurality of orthogonal PN codes in the memory device;

pseudo-randomly accessing the memory device to retrieve one of the plurality of PN codes, wherein each of the plurality of PN codes is associated with a useful life cycle before another PN code is pseudo-randomly retrieved; and

spreading a modulated data signal with the retrieved one of the plurality of PN codes.

2. (Original) A method as in claim 1 wherein the step of storing the plurality of orthogonal PN codes in the memory device further comprises the steps of:

storing unbalanced orthogonal PN codes in the memory device; and

storing balanced orthogonal PN codes in the memory device.

3. (Original) A method as in claim 2 wherein the step of storing unbalanced orthogonal PN codes in the memory device further comprises the step of storing Gold PN codes.

4. (Original) A method as in claim 1 wherein the step of pseudo-randomly accessing the memory device to retrieve one of the plurality of PN codes further comprises the steps of:

providing an addressable multiplexer;

coupling the addressable multiplexer to the memory device;

clocking a PN-code from the memory device to the addressable multiplexer;

pseudo-randomly selecting an input address of the addressable multiplexer; and

outputting from the multiplexer a PN-code associated with the selected input address.

5. (Original) A method as in claim 4 wherein the step of clocking the PN-code from the memory device further comprises the step of clocking the PN-code at a rate equal to a symbol rate.

6. (Original) A method as in claim 4 wherein the step of clocking the PN-code from the memory device further comprises the step of clocking the PN-code at a rate equal to a integer multiple of a symbol rate.

7. (Original) A method as in claim 4 wherein the step of pseudo-randomly selecting an input address of the addressable multiplexer further comprises the step of constraining the pseudo-random selection to select the input address based upon a previously selected one of the plurality of PN codes.

8. (Original) A method as in claim 4 wherein the step of pseudo-randomly selecting an input address of the addressable multiplexer further comprises the step of constraining the pseudo-random selection to select the input address based upon a previously selected input address.

9. (Currently Amended) A method as in claim 1 wherein the useful lifecycle comprises N symbol periods, where N is an integer ~~where N = 1,2,3,...~~ .

10. (Original) A method as in claim 1 wherein the step of spreading the modulated data signal with the retrieved one of the plurality of PN codes further comprises the steps of:

spreading a phase shift keying (PSK)modulated signal with the retrieved one of the plurality of PN codes for the useful life cycle associated with the retrieved one of the plurality of PN codes.

11. (Original) A pseudo-noise (PN) code hopping device, the device comprising:

at least one memory device, wherein the at least one memory device comprises:

a plurality of time limited PN codes;

an addressable multiplexer, wherein the addressable multiplexer is coupled to the at least one memory device; and

an address generator, wherein the address generator is coupled to the addressable multiplexer.

12. (Currently Amended) A PN code hopping device as in claim 11 wherein the at least one memory device further comprises:

a N-x-Spreading Factor (SF) storage capacity, where N is an integer equal to a [[=]] number of chips and SF [[=]] is equal to N/symbol; and

N-parallel outputs.

13. (Currently Amended) A PN code hopping device as in claim 11 wherein the at least one memory device further comprises:

a N-x-Spreading Factor (SF) storage capacity, where N is an integer equal to a [[=]] number of chips and SF [[=]] is equal to N/symbol;

a universal serial bus (USB) port; and
a serial to N-parallel converter.

14. (Currently Amended) A PN code hopping device as in claim 11 wherein the addressable multiplexer comprises a N:1 multiplexer where N is an integer equal to a [[=]] number of chips associated with one of the plurality of time limited PN codes.

15. (Original) A PN code hopping device as in claim 11 wherein the address generator comprises a look-up-table (LUT).

16. (Original) A PN code hopping device as in claim 11 wherein the address generator comprises a shift register.

17. (Original) A PN code hopping device as in claim 11 wherein the address generator comprises:

an up-down counter; and

a look-up-table, wherein the look-up-table is coupled to the up-down counter.

18. (Currently Amended) A ~~PN~~ pseudo noise (PN) code hopping system for mitigating cross-correlation interference between Direct Sequence-Code Division Multiple Access (DS-CDMA) users, the system comprising:

a first PN code hopping module, wherein the first PN code hopping module comprises:

a first memory device;

a first addressable multiplexer, wherein the addressable multiplexer is coupled to the first memory device;

a first address generator, wherein the first address generator is coupled to the first addressable multiplexer;

a second PN code hopping module, the second PN code hopping module is coupled to the first PN code hopping module, wherein the second PN code hopping module comprises:

a second memory device;

a second addressable multiplexer, wherein the addressable multiplexer is coupled to the second memory device; and

a second address generator, wherein the second address generator is coupled to the second addressable multiplexer.

19. (Currently Amended) A PN code hopping system as in claim 18 wherein the first memory device comprises:

a first modulation matrix M of size L x L, where L is an integer equal to [[=]] SF_{max}/SF_{min}, and where SF_{max} is a maximum spread factor and SF_{min} is a minimum spread factor and where SF_{max} and SF_{min} are integers, wherein the first modulation matrix comprises a first set of time limited PN codes; and

~~M^0-M^{L-1}~~ L parallel outputs.

20. (Currently Amended) A PN code hopping system as in Claim 18 wherein the first addressable multiplexer comprises a ~~M^0-M^{L-1}~~ L:1 multiplexer.

21. (Original) A PN code hopping system as in Claim 18 wherein the first address generator comprises:

a first up-down counter; and

a first look-up-table (LUT), the first LUT coupled to the first up-down counter.

22. (Original) A PN code hopping system as in Claim 18 wherein the first address generator comprises a first shift register.

23. (Currently Amended) A PN code hopping system as in claim 18 wherein the second memory device comprises:

a second modulation matrix (M) of size P x nP, where $P = SF_{max}/L$, where L is an integer [[=]] equal to SF_{max}/SF_{min}, where SF_{max} is the maximum spread factor and

SF_{min} is the minimum spread factor, where SF_{max} and SF_{min} are integers, a code order number n [[=]] is equal to a PN order, and wherein the second modulation matrix comprises a second set of time limited PN codes; and

~~G^0-G^{P-1}~~ P parallel outputs.

24. (Currently Amended) A PN code hopping system as in Claim ~~18~~ 23 wherein the second addressable multiplexer comprises a ~~G^0-G^{P-1}~~ P:1 multiplexer.

25. (Original) A PN code hopping system as in Claim 18 wherein the second address generator comprises:

a second up-down counter; and

a second look-up-table (LUT), the second LUT coupled to the second up-down counter.

26. (Original) A PN code hopping system as in Claim 18 wherein the second address generator comprises a second shift register.

27. (Currently Amended) A program storage device readable by a computing machine, tangibly embodying a program of instructions executable by the computing machine to perform method steps for mitigating cross-correlation interference, the ~~method~~ steps comprising ~~the steps of~~:

storing a plurality of orthogonal PN codes in ~~the~~ a memory device;

pseudo-randomly accessing the memory device to retrieve one of the plurality of PN codes, wherein each of the plurality of PN codes is associated with a useful life cycle before another PN code is pseudo-randomly retrieved; and

spreading a modulated data signal with the retrieved one of the plurality of PN codes.

28. (Currently Amended) A pseudo noise (PN) ~~PN~~ code hopping method for mitigating cross-correlation interference between adjacent cells, the method comprising the steps of:

providing a first set of PN spreading codes, the first set of PN spreading codes comprising:

a first subset of hoppable PN codes;

a second subset of non-hoppable PN codes, wherein the second subset of non-hoppable PN codes is used for system control purposes, the second subset of non-hoppable PN codes comprising:

at least one PN spreading code;

providing a memory device;

storing the first set of PN codes in the memory device;

pseudo-randomly accessing the memory device to retrieve one of the first subset of hoppable PN codes;

spreading a modulated data signal with the retrieved one of the first subset of hoppable PN codes.

29. (Original) A method as in claim 28 wherein the step of spreading the modulated data signal further comprises the step of spreading the modulated data for a time substantially equal to an integer multiple of a symbol time.